



# AMBA 3 APB® nVS

nSys Verification Suite

Verification IP

The **AMBA APB nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of AMBA 3 APB designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their AMBA APB compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

## Features

- ◆ Compliant to AMBA APB Protocol
- ◆ Support for all types of AMBA APB devices
  - Master
  - Slave
- ◆ Support for programmable wait states
- ◆ Configurable transfer size for read & write transactions
- ◆ Flexibility to send completely configured data
- ◆ Ability to inject errors during data transfer
- ◆ On-the-fly protocol & data checking

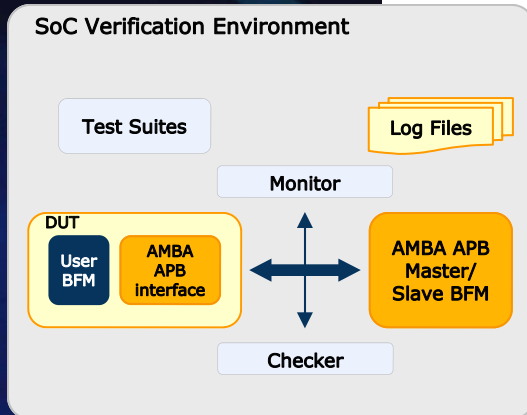
## nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Others**: SDIO, UART, I<sup>2</sup>C, SMBus, ASI, PCMCIA, IEEE1284

## Components

- ◆ AMBA APB Master/Slave BFM
- ◆ AMBA APB Checker
- ◆ AMBA APB Monitor
- ◆ Test Suites
  - Basic tests
  - Error tests
  - Directed tests
  - Constrained Random tests
  - User Specified tests

**World's largest portfolio of Verification IPs**



## Key benefits

- ◆ Faster & complete verification of AMBA APB designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

## Deliverables

- ◆ Validated AMBA APB Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

## Applications

- ◆ Standalone AMBA APB core or IP verification
- ◆ Verification of SoC with AMBA APB interface

## Other features

- ◆ Generating & driving bus traffic as a AMBA APB Master
- ◆ Responding to transactions as a AMBA APB Slave
- ◆ Mailboxes for data checking
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Option for SystemVerilog (OVM/VMM) & Verilog
- ◆ **Option for Unlimited/Licensed Source code licenses**
- ◆ Consistency of interface, installation, operation & documentation across nVS family

## Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

## About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

## About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.