

AMBA 3 AXI[®] nVS

nSys Verification Suite

Verification IP

The **AMBA 3 AXI nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of AMBA 3 AXI designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their AMBA 3 AXI compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design, and to verify their differentiators easily. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI[™] Family** : PCI Express[®]Gen3/Gen2/Gen1, SR-IOV, PCI-X[™], PCI[™]
- ☑ **Communications**: Ethernet (100/40/10/1G), Interlaken, SPI 4.1
- ☑ **Consumer**: USB 3.0, USB 2.0
- ☑ **Storage**: SAS, SATA 3.0, ATAPI
- ☑ **ARM AMBA[®]** : AXI, AHB, APB
- ☑ **Memory**: DDR3, DDR2
- ☑ **Others**: SDIO, I2C, UART, SMBus...

Features

- ◆ Support for all types of AMBA AXI devices:
 - Master
 - Slave
- ◆ Configurable transfer size for read & write transactions
- ◆ Configurable wait states on different channels
- ◆ Flexibility to send completely configured data
- ◆ Ability to inject errors during data transfer
- ◆ Support for Interconnect and Bridge
- ◆ Support for SASD, SAMD & MAMD buses
- ◆ Configurable default values for control signals
- ◆ Low power support
- ◆ **Available in native SystemVerilog (OVM/VMM) & Verilog**
- ◆ **Option of Source Code**

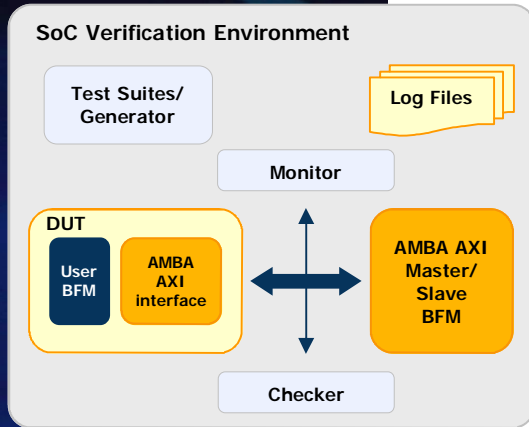
Components

- ◆ AMBA 3 AXI Master/Slave BFM
- ◆ AMBA 3 AXI Checker
- ◆ AMBA 3 AXI Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - **Functional Coverage tests (optional)**

World's largest portfolio of Verification IPs

AMBA 3 AXI® nVS

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Key benefits

- ◆ Coverage Driven Verification
- ◆ Faster & complete verification of AMBA 3 AXI designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated AMBA AXI Verification Suite: BFM, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone AMBA 3 AXI core or IP verification
- ◆ Verification of SoC with AMBA 3 AXI interface

Other features

- ◆ Generating & driving bus traffic as a AXI Master
- ◆ Responding to transactions as a AXI Slave
- ◆ Support Write data interleaving
- ◆ Support Out of order transactions
- ◆ Supports unaligned data transfer
- ◆ Support for multi-master & multi-slave configuration
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Consistency of interface, installation, operation & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the World's Largest Portfolio of Verification IPs to provide products and services that Accelerate designs of customers developing ASIC/ SoC, while lowering their costs & risks.

About nVS

nVS (nSys Verification Suite) family of VIPs is integrated to work with popular languages, like, 'e', SystemC, OpenVera, VHDL, on all commonly used simulators/platforms. nVS is a complete Verification IP solution for pre-silicon Functional Verification of ASIC/SoC designs.



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**Product
Evaluation**

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