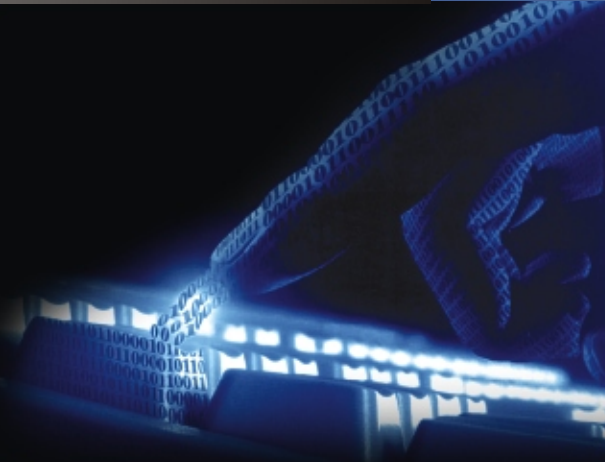


Introduction

The Advanced Switching Interconnect (ASI) nVS is a comprehensive solution for functional verification of ASI devices. The nVS allows design and verification engineers to quickly and extensively test the entire functionality of their ASI compliant devices. Availability of Test Suites enables the designer to focus on features unique to his design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.



nVS Family

- PCI Express
- PIPE based PHY
- ASI
- DDR2
- PCI-X
- SATA
- Others: ATAPI, PCMCIA, PCI, IEEE1284, UART

Features

- Built upon the proven and widely accepted nVS for PCI Express
- Support for all types of ASI devices
 - ASI Endpoints
 - ASI Switch
- Support for all complementary protocols
 - SLS: Simple load/store
 - SQs: Simple queuing
 - SDT: Socket data transport
 - P18: PCI Express-ASI Bridge
 - User defined
- Flexibility to send completely automated packets or completely user configured packets in all the layers
- Ability to inject errors in packets being generated in all the layers
- Support for all Link widths And PHY interfaces

Overview

Components

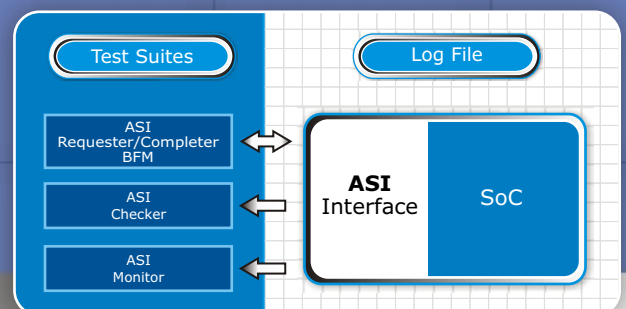
- ASI Requester/Completer BFM
- ASI Checker
- ASI Monitor

Test Suites

The ASI nVS provides following Test Suites:

- Basic tests
- Error tests
- Compliance tests
- Directed tests
- Constrained Random tests
- User specified test cases

SoC Verification Environment



Benefits

- Ensure compatibility and compliance of ASI designs without writing a single line of code
- Significant improvement in Verification productivity
- Lower rate of failure/re-spin

Other Features

- Based upon Advanced Switching Core Architecture Specifications Revision 1.0
- Generates and responds to transactions
- Support for:
 - Multicast and Unicast packets
 - Path building
 - Congestion Management
- Implements ASI Device configuration space
- Implements PCI Express configuration space as defined for End Points & Express Extended Capabilities Configuration Space registers as well as PCI Express Advanced Error Reporting Capabilities register.
- Simple and flexible BFM tasks
- Ability to send raw user defined packets
- Fully Automated Flow Control
- Support for ASI superset functionality to the Link Layer specification
- Highly parameterized: Verification environment & Logical parameters
- Mailboxes for data checking
- Programmable message logging capabilities
- Available in Verilog for all major simulators and for all major platforms.

Deliverables

- Validated ASI verification suite
- User Manual and release
- Test Suites

Applications

- Standalone ASI IP or core verification
- Verification of SoC with ASI interface

Support

nVS family of Verification IPs is backed by a dedicated team of engineers trained in advanced verification methodologies, with a track record of excellent customer support. Customers can choose from a variety of support options from e-mail, phone or onsite.

About nSys

nSys provides products & services to Accelerate Designs of its customers, by focusing on the verification phase of ASIC development. nSys offers nVS family of products for industry standards. nSys also offers services for development of Verification IPs, for other standards or for customers' proprietary interfaces.

About nVS family

nSys Verification Suite (nVS) is a complete verification solution consisting of BFMs, Checker + Monitor and Test Suites for standard interfaces and protocols. The nVS family provides the same consistent user interface across industry standards, simulators and verification environments. The nVS family also offer consistency of installation, operation, and documentation. The nVS family supports a large number of protocols and standards, that enable users to quickly build a system-level environment to verify their advanced SoC designs without having to write a single line of code.



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