

# ASIC/ FPGA/ IP Design Services

Time-to-market pressures and the need for integrating more functions in silicon is fueling the SoC market's growth. At nSys, we leverage systems knowledge, experience with technologies like PCI Express & ARM, proven Verification IP portfolio and optimized Intellectual Property components in areas such as:

- ◆ Memory, FIFO, Stack
- ◆ Data Integrity
- ◆ Logic, Counters
- ◆ DSP
- ◆ BIST, JTAG

nSys offers ASIC/ FPGA/ IP design service that encompass architecture and design to implementation, synthesis and silicon validation to help Accelerate designs while greatly increasing the possibilities of success and finally translates upto 40% faster time-to-market.

## Services

- ASIC/ FPGA/ IP Design services**
- Independent Verification services**
- SystemVerilog Migration services**
- Post Silicon Validation services**

## Why nSys?

- ◆ Extensive experience in providing Product development services in the area of ASIC/ FPGA/ IP design & verification
- ◆ Rich library of proven Intellectual Property components that can be quickly plugged into any system design
- ◆ Leverage nSys Verification Suite (nVS) family, the world's largest portfolio of Verification IPs
- ◆ Experience in independent verification
- ◆ Experience in targeting several Synthesizable Verilog & VHDL models to ASIC/ FPGA
- ◆ Transparent Project Management
- ◆ Proactive and responsive engineering team
- ◆ User friendly project portal
- ◆ Flexible business models
- ◆ Ability to deploy resources at a very short notice

## Capabilities

- ◆ Architecture definition
- ◆ RTL coding in Verilog/ VHDL
- ◆ Synthesis and netlist generation
- ◆ Static timing analysis and timing extraction

**World's largest portfolio of Verification IPs**

## Sample Projects:

- ASIC/IP development
  - ◆ PCI-X to PCI Fault tolerant Bridge
  - ◆ PCI to PCI Bridge
- FPGA
  - ◆ Altera: PCI-X core
  - ◆ Xilinx: 3G module

## Key Benefits

- ◆ Significant improvement in development productivity
- ◆ Lower rate of failure/ re-spin
- ◆ Reduced time to market

## Deliverables

- ◆ Source code of RTL, Testbenches, Test Suites
- ◆ RTL netlist targeted to selected foundry
- ◆ Synthesis scripts
- ◆ Design Documents
- ◆ Verification Plan and report

## Applications

- ◆ Architecture to GDS-II
- ◆ RTL development & verification
- ◆ RTL to GDS-II
- ◆ FPGA prototyping of SoC/ ASIC Verification
- ◆ FPGA-to-ASIC Translation
- ◆ FPGA-to-FPGA Translation
- ◆ RTL Optimization for Timing/Area/FPGA
- ◆ IP implementation

## Key Milestones

- ◆ Customer Requirement Specifications
- ◆ Project Development Plan
- ◆ Architecture & design
- ◆ Verification Plan
- ◆ RTL and Test Environment coding
- ◆ Execute Verification Plan
- ◆ Synthesis and Timing closure
- ◆ Acceptance

## About nSys

nSys is the leading provider of Verilog and VHDL based Verification IPs. nSys provides products & services to Accelerate Designs of its customers, by focusing on the verification phase of ASIC development.

## About nVS family

nSys Verification Suite (nVS) family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA/IP developers in over 10 countries are currently using the nVS family and benefit from widely accepted & proven Bus Function Models, Monitors, Assertions-based Checkers and Test Suites for standard interfaces/protocols, that enable users to quickly build environments to verify their designs at system as well as block levels.



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