



Ethernet nVS

nSys Verification Suite

The **Ethernet nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of 10G/1G Ethernet interface designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their Ethernet compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI®** : PCI Express®, PCI-X®, PCI
- ☑ **ARM® AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet (10G/1G), USB 2.0, SPI 4.2
- ☑ **Memory**: DDR3, DDR3
- ☑ **Others**: SDIO, PCMCIA, IEEE1284, UART, I²C, SMBus

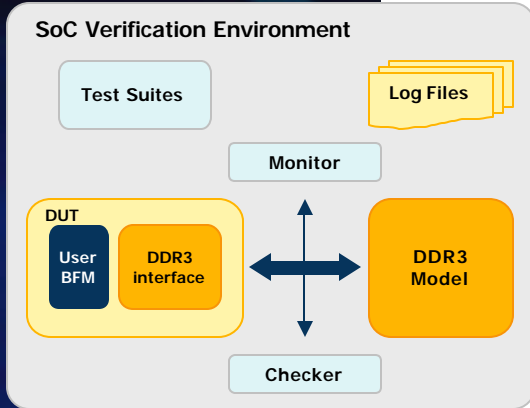
Features

- ◆ Full timing, bus functional modeling of IEEE 802.3 (2005) specifications
- ◆ Support for XGMII, XAUI, GMII interfaces
- ◆ Supports 10Gb/s & 1Gb/s
- ◆ Full/Half (1G) Duplex Flow Control support
- ◆ Supports frame types: Data & Control Pause
- ◆ Automatic re-transmission of Control Pause frame
- ◆ Link State Fault generation mechanism
- ◆ Supports collision scenarios and implements back-off algorithms (1G)
- ◆ On-the-fly protocol & data checking

Components

- ◆ Ethernet MAC BFM (XGMII, XAUI, GMII)
- ◆ Ethernet Checker
- ◆ Ethernet Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Constrained Random tests
 - User Specified tests

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster and complete verification of DDR3 designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated DDR3 Verification Suite as encrypted/licensed source code
- ◆ User Manual and Application notes
- ◆ Test Suites in source code

Applications

- ◆ Standalone DDR3 core or IP verification
- ◆ Verification of SoC with DDR3 interface

Other features

- ◆ Monitor and Checker are independent modules and can be used with other vendors' memory models
- ◆ Back door access to memory locations
- ◆ Generates detailed Assertion coverage report
- ◆ On-the-fly protocol and data checking
- ◆ Available in Verilog, SystemVerilog
- ◆ Consistency of interface, installation, operation, and documentation across nVS family

Support

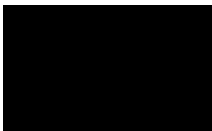
nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys leverages the world's largest portfolio of Verification IPs it has developed, to provide products & services to Accelerate Designs for its customers developing ASIC, FPGA or IP.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA/IP developers in over 10 countries are currently using the nVS family & benefit from widely accepted & proven Bus Function Models, Monitors, Assertions-based Checkers & Test Suites for standard interfaces/protocols, that enable users to quickly build environments to verify their designs at system as well as block levels.



Accelerating designs

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