From Concept to Completion: The Power of Custom SoCs and End-to-End Synopsys Solutions

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Introduction

With the ever-increasing new technologies and innovations in Artificial Intelligence (AI), Machine learning (ML), Virtual/Augmented reality, and the enormous amount of data generated from all connected devices, there is a lot of demand for High-performance computing and customized chip design solutions. This drives the need for custom silicon hardware development tailored for customized workloads in the data center to manage the ever-growing need for compute performance, performance per milli-Watts, and the total cost of ownership (TCO) in data centers.

On top of this and with the slowdown of Moore's law, there is great innovation in 2.5D and 3D packaging technologies to stack multiple chips or chiplets in the same package and die-to-die interfaces like UCIe.

In this paper, we discuss why custom SoCs are designed, what it takes to build one, and how Synopsys can help to realize it.

Why Create a Custom SoC?

To meet the complexity of the system-on-chip within the given time frame, companies must move fast to tackle the insatiable need for custom silicon targeted for different applications and market segments.

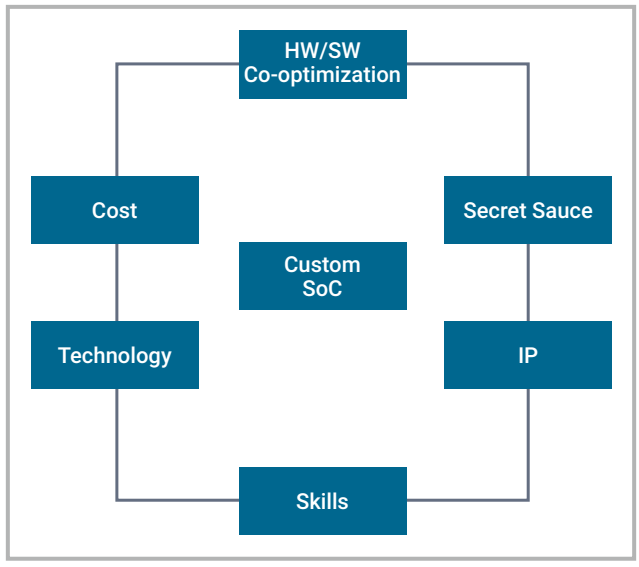


Figure 1: Justifications for custom SoC

- **Hardware and Software co-optimization:** More and more companies are driving a vertical development model where software and hardware are being developed hand-in-hand to get an optimized and scalable solution. This is where architecture modeling with Synopsys Platform Architect™ (PA), software development, and bring-up using Synopsys ZeBu® and Virtualizer™ are key for co-optimizing software and hardware
- **Secret Sauce/Differentiation:** With more and more customers creating innovative solutions for AI, ML, Data Centers, Automotive, Accelerators, etc., the need for custom solutions is higher than ever. Each customer's product usually has a secret sauce in the form of an IP or an FPGA solution, or a software algorithm that differentiates their IP from the competition. To realize that into a product, we must create a SoC around the IP with standard interfaces like DDR, Interconnect IP, PCIe, UCIe, DisplayPort, I2C, UART, SPI, etc.
- **IP/SerDes:** The fact that most designs use standard IPs like DDR, PCIe, Ethernet, etc., having these IPs readily available for SoC integration is key to managing risk and scheduling. The content of IP/SerDes continues to grow in IC development based on bandwidth and overall latency requirements, driving complex IP development in new technology nodes. IP ecosystem is one of the critical components in SoC development
- **Technology know-how:** When customers decide on a process node based on their PPA targets, the SoC development team must have expertise in the process node for development, as the selected node could be challenging for several reasons. Some of the typical challenges include MHz/mV not meeting the requirement, leakage or power targets not meeting the target, die size being too big in the chosen node, etc. Having the know-how in EDA implementation flows and methodology, IP design and process design flow design technology co-optimization (DTCO) is key for the end-to-end SoC development in new nodes. Synopsys technology portfolio provides the complete solution from DTCO and process implementation to architecture modeling and software bring-up, IP eco-system, and EDA tools. It flows as a one-stop shop for customers
- **Skills augmentation:** Customers need secondary and sometimes primary resources with skills like RTL development, verification, DFT, and physical design. For custom SoCs, the composition of the customer's expertise is the key to building a custom design. With a custom IP design and specific needs for enabling and testing the IP, Synopsys provides a diverse spectrum of tools and skills required for the customer to complete the design and test the IP. This helps augment the customer's skills, from early architecture analysis and RTL development to verifying the design and implementing the design to the tapeout. We also offer flexible business models to fit the customer's needs
- **Cost of development:** SoC development costs have been skyrocketing for years, and with challenges like chip shortages, acquiring resources and wafers for chips has been a challenge. Putting an SoC team together for the sake of a custom SoC development is a monumental task and it takes up a lot of time. With Synopsys augmentation, customers can take advantage of the expert resources to help speed up the development and in turn reduce the overall cost of development of SoCs

What Does It Take?

Ecosystem and Operating Space

We enable our customers in HPC, client, server, mobile, automotive, aerospace and government, IoT, etc. The requirements and specifications for all these areas demand various tools, flows, methodologies, design expertise, and subject matter experts (SME).

Tools: Synopsys leads the way providing the required tools to design chips in the above-mentioned operating spaces

Methodologies: For each area of chip design, reference methodologies are developed to enable the tools and the corresponding flows

Design: We have expertise in chip design for various markets that include, but are not limited to, mobile, client, server, automotive, and others

SME: Our subject matter experts can drive the design, tools, flows, and methodologies and can collaborate with the customers to reach the relevant goals

EDA Leadership—Tools

Synopsys is the leader in providing the necessary tools and flows to build the best-in-class SoCs, from IP integration to building a custom SoC.

System Solutions

Along with the tools and flows, the various solutions required for a custom SoC can be supplied for all the critical areas that include architecture analysis, emulation/prototyping, RTL development and integration, DFT, physical design, firmware development, along with the coordination of tapeout management with our manufacturing service partners.

How?—The Approach

SoC Flows and Infrastructure

An example flow (Figure 2) is used to deliver SoC solutions to our customers. We create flows required for the most efficient use of the tools and partners with manufacturing service providers (MSP) to provide complete solutions to customers.

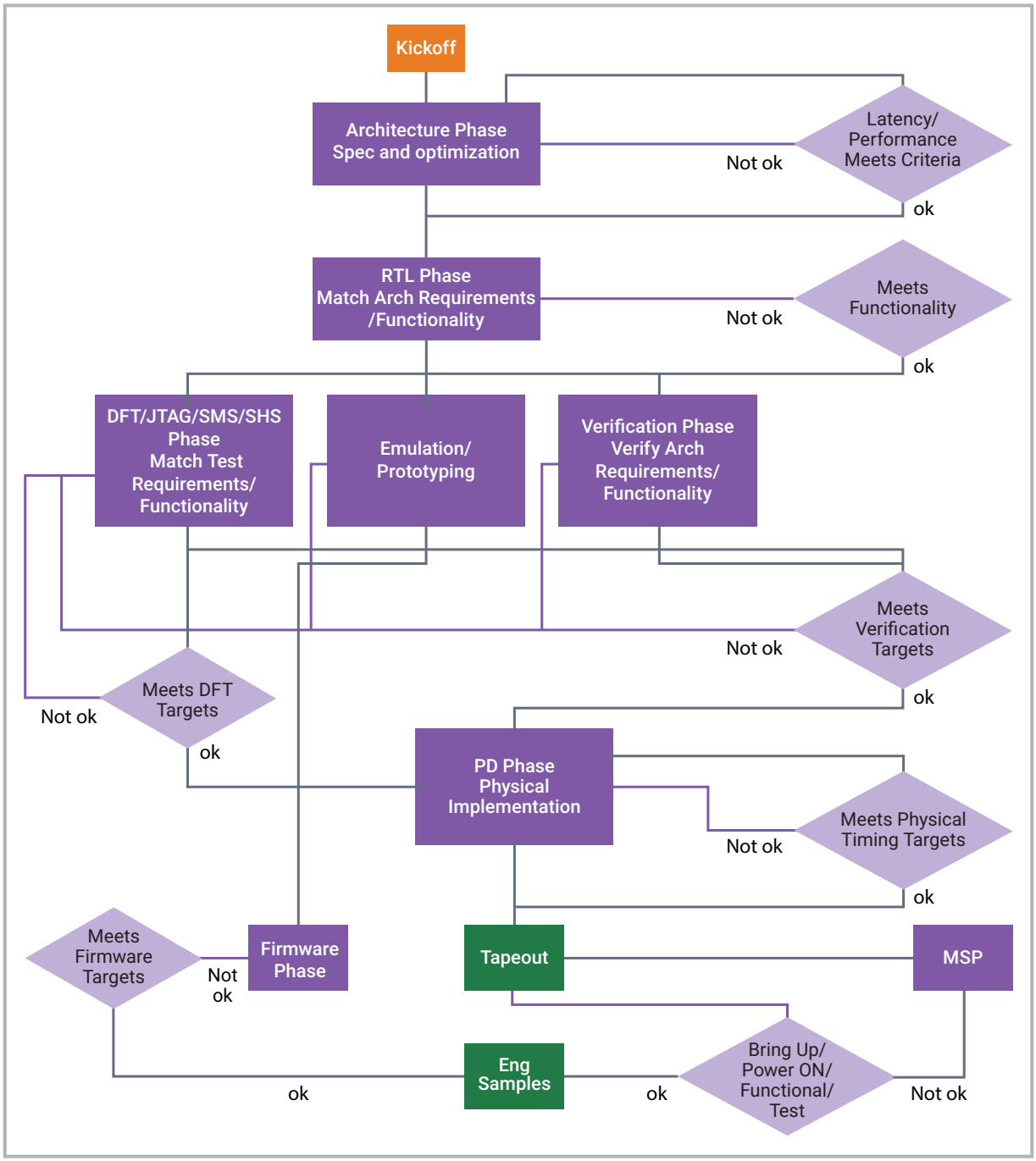


Figure 2: Example SoC flow

1. Architecture

Synopsys assists customers with both early architecture feasibility studies as well as analyzing a pre-defined architecture. We collaborate closely with the customers to define their SoC architectures. Early architecture analysis includes the following:

- High-level feature alignment
- Commercial vs. automotive vs. aerospace feature alignment
- Workloads to be targeted and derive performance goals
- System IP selection and readiness
- IO and peripheral IP selection
- Technology readiness
- Package selection for SoC (monolithic vs. chiplets)
- Power projections and power dashboard
- Performance projections and thermal considerations
- Area dashboard
- Architecture analysis for performance and bandwidth
- RTL Design and micro-architecture definition of all sub-systems
- Verification plan—pre-silicon, emulation, and prototyping as needed
- Firmware development
- Design for testability (DFT) architecture, implementation, and post-silicon vector generation
- Schedule and resource planning

In the case of pre-defined architecture, we assist customers in analyzing the SoC architecture development phase with Platform Architect in terms of bandwidth and performance analysis, along with using representative workloads for early software development and testing using Virtualizer.

Expertise in this area can help shift left the RTL development and early software development. Quick iterations with various IP configurations can be analyzed with Platform Architect to commit to a suitable SoC architecture.

An initial IP configuration with a desired performance and bandwidth can be generated to assist with the RTL development.

2. RTL

Once the initial IP configuration is defined from the architecture phase, an initial SoC RTL can be generated to enable the downstream flows for DFT, verification, emulation, prototyping, firmware, and physical design.

Custom RTL for components like Clocks, Resets, Padring, and any specific functional blocks required for the SoC will have to be created based on the project-specific goals.

With Core-Consultant/Core-Assembler solutions, IPs can be integrated seamlessly and generate high-quality SoC RTL. Testbenches required for quick verification are automatically generated along with constraints for quick synthesis and spyglass lint/CDC checks. The key RTL tasks primarily include:

- Micro-architecture for sub-systems and SoC Top Level
- RTL coding and integration
- Constraints development
- Unified power format (UPF) development
- DFT integration
- Verification
- Gitlab releases for tracking
- Bug fixes after functional verification

3. DFT

Synopsys offers SoC DFT architecture and implementation solutions, along with flows for TestMax, key DFT features like scan, B-scan, SMS/SHS, XLBIST for integration. Along with the above features, Synopsys IP will include scan wrappers for DFT, and patterns will be generated to ensure the test coverage meets the requirements.

The key DFT tasks primarily include:

- Scan Architecture along with all essential DFT, including boundary scan, scan chains, core wrapping, test points, and compression
- On-chip Clock Controllers for controlling various DFT modes.
- Test point insertion to improve coverage
- MBIST for memory testing with STAR Memory System/STAR Hierarchical System (SMS/SHS)
- Automated test integration and validation of all IP/cores, including mixed-signal IP on SoC using STAR Hierarchical System
- LBIST for automotive applications
- Meet overall stuck-at and transition coverage targets

4. Verification

The verification of the SoC can be broken into three distinct areas:

- Functional simulations
  - VCS-based simulations to ensure that the Synopsys IP and SoC created is fully functional
  - A verification plan along with functional and code coverage targets for each of the sub-systems and SoC will enable the design to be fully verified and reduce the possibility for post-silicon bugs
- Emulation
  - Emulation is much faster with simulation acceleration than with VCS, and typical use cases are boot flow verification, Display or PCIe verification, etc.
  - With the Zebu transactors, SoC verification can be started early while waiting for sub-systems to be ready for full-chip verification
  - Zebu emulator will enable software-driven SoC debug and design
  - For a given subsystem or a full SoC, a Zebu emulation model can be created to enable software development as soon the initial RTL is ready
- Prototyping
  - Prototyping is very handy for testing any hardware that may be attached to the SoC, especially IO interfaces. Synopsys HAPS® can help customers to realize the full system along with the SoC development and ensure all peripherals are assembled correctly in the customer environment

The overall goal is to verify the design thoroughly and reduce any post-silicon surprises, as well as reduce chip revisions. The coverage goals and testing criteria will help to reduce the possible cracks in the design verification. The verification coverages are broken into two groups:

- Functional Coverage
  - Core or block-level tests
  - Subsystem and SoC-level tests
- Code Coverage (Merged)
  - Line
  - Condition
  - Toggle
  - Branch

5. Physical Design

Once RTL is verified, it is released to the physical design team for implementation. Our team has expertise in implementing designs for all major foundry technologies and for various design styles.

The key physical design tasks primarily include, but are not limited to the following:

- Floorplan/Design planning
- Package/die feasibility and 3DIC planning for chiplets
  - Closely work with manufacturing services provider for packaging/silicon bring-up/post-silicon
- Synthesis
- DSO.ai™ for PPA targets
- Low power design implementation
- Place and route
- Timing closure
- Physical verification
- Formal verification
- IR/EM/ESD analysis

Along with the primary tasks of the physical design closure, we do extensive PPA studies that yield the best possible performance per Watt.

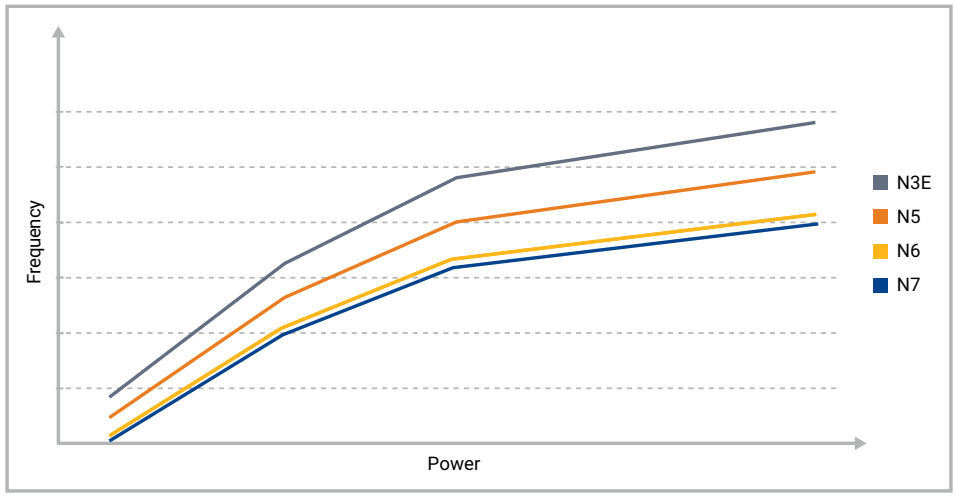


Figure 3: Performance vs. power across process technology nodes

6. Firmware

Synopsys Design Services assists our customers with firmware development on custom SoCs. As shown in the flow chart in Figure 2, HAPS and ZEBU are used in the development of the firmware.

The key firmware tasks primarily include:

- Boot code development
- Chip configuration and control
- Power management
- Security
- Design verification using HW/SW co-verification
- Silicon bring-up and post-silicon validation

Partnerships

We have partnered with industry leaders to deliver chips in their representative product segments.

- Technology development and foundry interface—TSMC, Samsung, and GlobalFoundries to name a few
- Manufacturing service providers such as GUC, Alchip, SiFive, CAES (Frontgrade Technologies now)

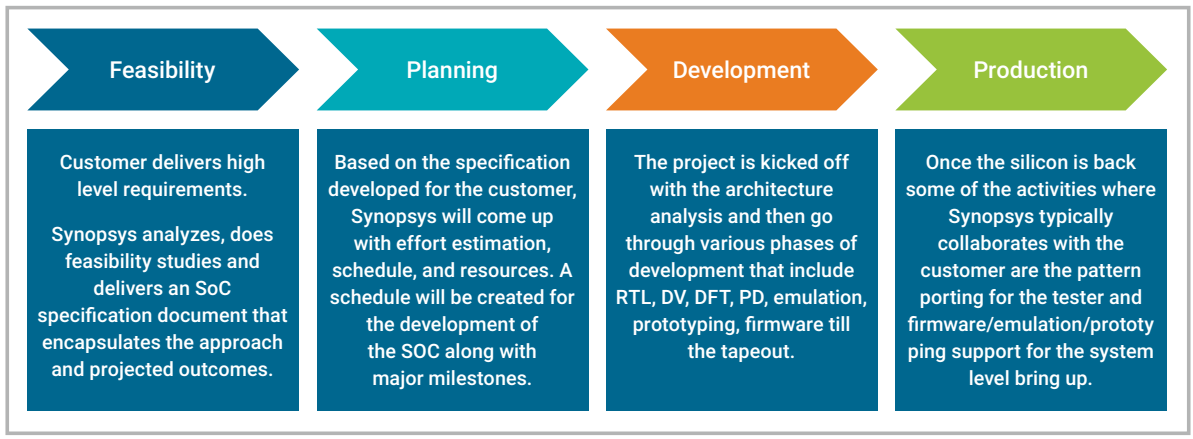
Our custom SoC solution involves planning with the MSP and foundry to deliver the final packaged parts.

SoC Development Life Cycle

The development of SoC can be broken into four distinct phases.

- Feasibility
- Planning
- Development
- Production

Let us look into the key tasks involved in these phases of the SoC design cycle.



Next Generation of SoC Designs

With the slowdown of the Moore's law, SoC designs are evolving into more of system of systems. This is being made possible by various chiplet-based architectures. The demand for more features in SoCs is fueling the need for chiplet-based architectures to fit in each system.

Synopsys 3DIC compiler helps in planning, design, implementation, and the overall integration of chiplets. With the right tools and expertise, our custom SoC development team can accelerate the development of next-generation SoCs.

Call to Action

The key differentiation that we offer in custom SoC development is access to robust EDA solutions and a strong IP portfolio for solving complex chip design problems augmented with powerful Engineering Talent.

Time-to-market is the key to the success of our customers. With the help of our tools and engineering talent, we enable our customers to bring their products to the market faster.

Emerging technologies like AI/ML, where we have been heavily investing (e.g. Synopsys DSO.ai™), will help to reduce iterations in the chip development and save the mounting costs of the development.

We invite you to join us for the continued success of your products and solutions in SoC development.

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