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Synopsys Design Compiler NXT

2X faster runtime, superior quality-of-results, and a new cloud ready distributed processing engine

Overview

Synopsys Design Compiler® NXT is the next step in the evolution of the industry leading Synopsys Design Compiler family. Building on the industry-standard Synopsys Design Compiler Graphical to continue delivering innovative synthesis technology, Synopsys Design Compiler NXT delivers 2X faster runtime and superior quality of results (QoR). The technology links from Synopsys Design Compiler Graphical into Synopsys IC Compiler™ II are further strengthened to tighten timing, parasitic resistance, and capacitance correlation between synthesis and place-and-route. Synopsys Design Compiler NXT synthesis technology is enabled for next-generation process node technologies, including below 5nm.

Key Benefits

- Builds on the benefits of Synopsys Design Compiler Graphical by enabling a new, advanced feature set to improve designer productivity and yield better QoR at the most advanced design nodes
- Plug-and-play, user interface (UI), and script compatible with Synopsys Design Compiler Graphical
- 2X faster runtime, with improved multi-threading technology for better scalability up to eight CPUs
- 12% lower total power and 10% smaller area QoR through advanced optimizations and concurrent clock and data (CCD) technology
- Next-generation process node support, including below 5nm
- Enhanced physical guidance to Synopsys IC Compiler II, with improved RC and timing correlation
- Shares a common library and block abstract models with Synopsys IC Compiler II, while retaining support for the Synopsys MilkyWay™ library format

2X Faster Runtime

Significantly faster runtime accelerates design closure for even the most technologically advanced integrated circuit (IC) designs. Inside Synopsys Design Compiler NXT, core engine speed-ups improve runtime across a wide variety of customer designs and achieve better scalability up to eight cores by using a new intelligent multi-threading technology to further enhance runtime across all synthesis optimization stages. This approach enables further speed-ups, which are particularly beneficial for the larger design sizes found at advanced nodes without sacrificing any QoR trade-off.

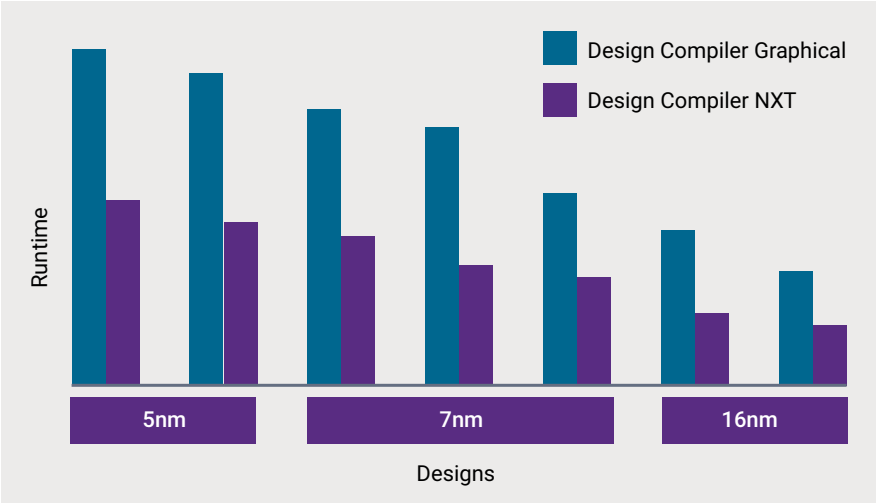

Figure 1: Design Compiler NXT runtime improvement

Better Quality-of-Results

New optimizations yield 10% smaller area and 12% total power savings. New techniques are introduced for mapping, restructuring, rewiring, and other operations to reduce dynamic power without degrading timing, area, or congestion. Deployment of concurrent clock and data (CCD) optimization technology from Synopsys IC Compiler II improves timing and power recovery through dynamic management of skew.

Enablement Across all Leading-Edge Process Nodes

Synopsys Design Compiler NXT is the leader in synthesis for advanced nodes down to and below 5nm. Leadership at advanced nodes is maintained with continued support for via pillars, pattern must join, auto non-default rule (NDR), pin access-awareness, variant-aware libraries, layer-aware optimization, and other requirements. New synthesis capabilities are constantly in development to support ever-evolving foundry requirements to meet customer expectations of the performance, power, and area (PPA) benefits derived from the next-generation production process node in development.

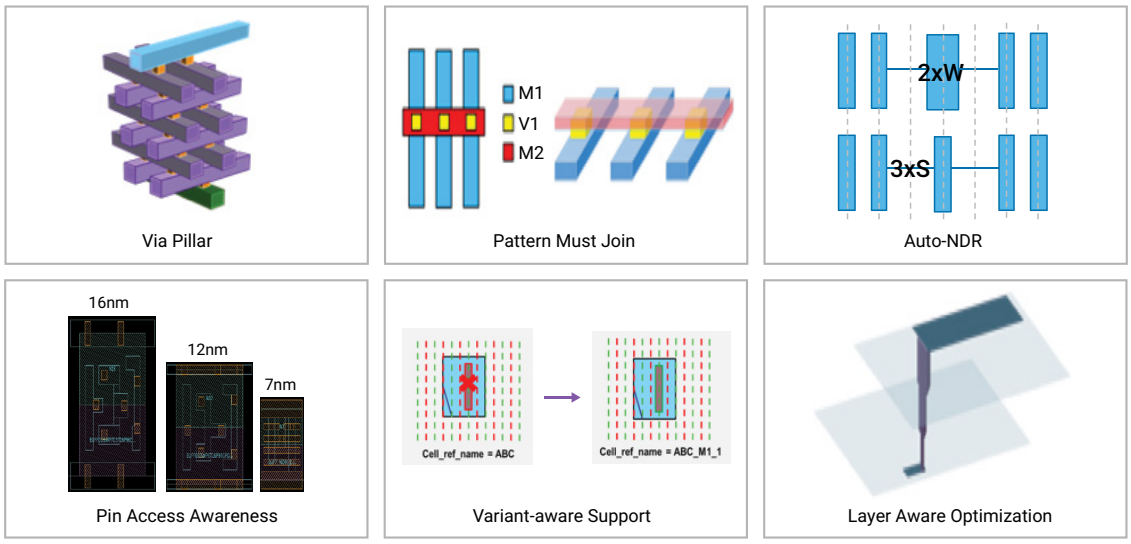

Figure 2: Advanced process node support

Enhanced Physical Guidance to Synopsys IC Compiler II

With designs becoming larger more complex at smaller geometries, RTL designers require an even tighter correlation between synthesis and layout results. To achieve the most efficient RTL-to-GDS flow, parasitic estimations of net topology are aligned between Synopsys Design Compiler NXT and Synopsys IC Compiler II, such as unit RC modeling and via estimation, while also considering local density during the parasitic calculations. The correlation between synthesis and place-and-route is further improved by using high-accuracy timing models for path-by-path and endpoint-by-endpoint calculations.

Common Library and Block Abstract Models

Synopsys Design Compiler NXT users benefit from sharing a common library and block abstract models with Synopsys IC Compiler II because they can use the same libraries for both synthesis and place-and-route. If library models are updated as a design is still under development, then there is a reduced risk that libraries will get out of synchronization between synthesis, place-and-route, and physically-aware signoff-driven ECO design phases.

Building on the Capabilities of Synopsys Design Compiler Graphical

- Synopsys Design Compiler NXT is plug-and-play, UI and script compatible with Synopsys Design Compiler Graphical
- Cross-probing between RTL and design views such as schematic, timing reports, and physical views for faster debugging
- QoR metrics visualization can help quickly identify design issues and compare results from multiple sessions
- Early physical visualization and debugging identify layout issues prior to physical implementation
- Floorplan exploration for faster design convergence to an optimal floorplan
- Accurate pre- and post-synthesis congestion prediction and congestion-driven optimization eases routing
- Gate-to-gate optimization for smaller areas on new or legacy designs while maintaining timing QoR
- Concurrent multi-corner, multi-mode (MCMM) synthesis

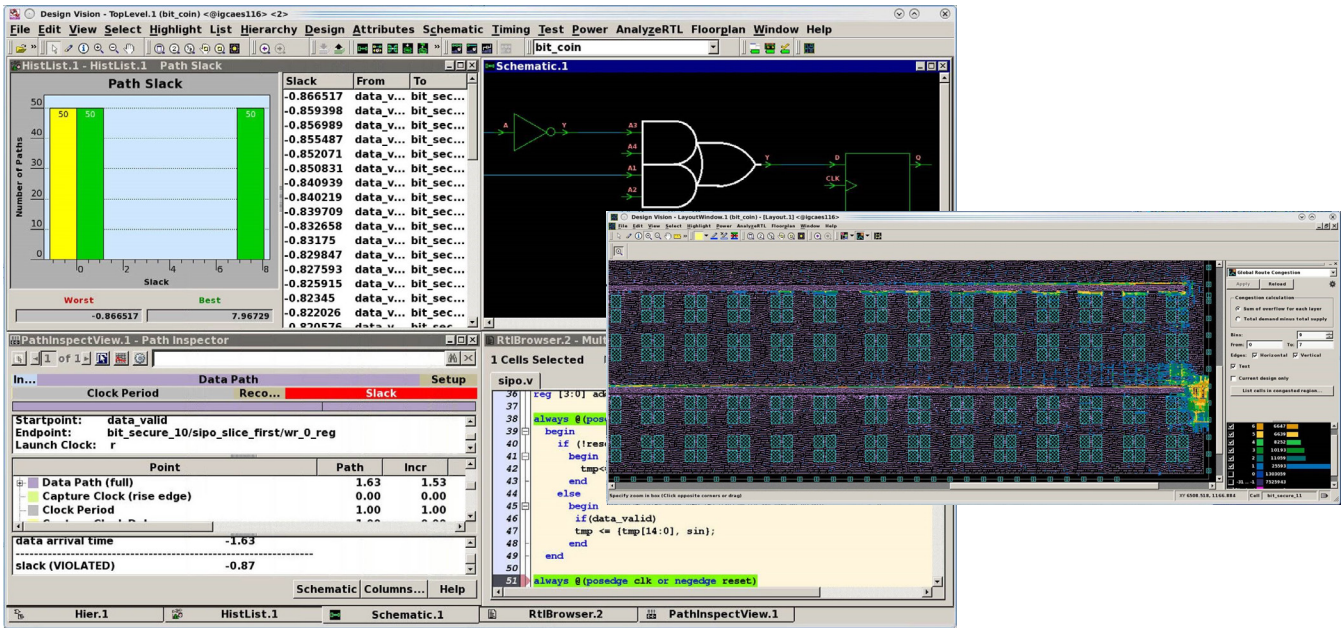

Figure 3: Cross-probing between RTL, schematic, timing, and layout views

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