TestMAX XLBIST

X-Tolerant Logic Built-in Self-Test (BIST)

In-system self-test for safety critical designs including automotive, medical, and aerospace

Overview

Synopsys TestMAX XLBIST delivers a solution for in-system self-test of digital designs where functional safety is critical, such as in automotive, medical, and aerospace applications, and is the industry's first X-tolerant architecture (Figure 1) that eliminates all Xs in a design. The result is smaller impact on test costs and faster time to market.
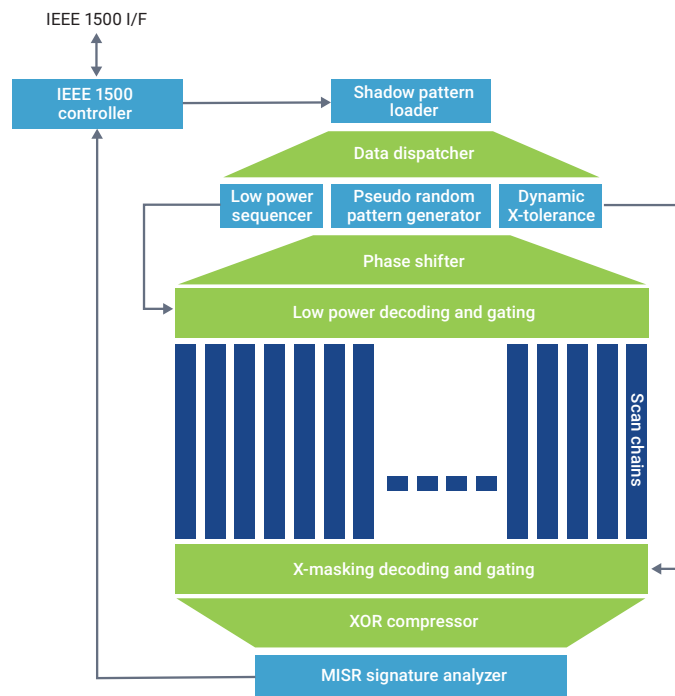

Figure 1: TestMAX XLBIST architecture overview

Key Benefits

- Addresses ISO 26262 automotive functional safety and other in-system test requirements
- Predictably achieves target test coverage within given run time, clock frequency, and power constraints
- X-tolerant logic BIST eliminates designer effort to address unknown logic values (Xs)

Key Features

- Supports standard and high X-tolerance architectures
- In combination with TestMAX ATPG, supports deterministic compressed patterns
- Intelligent re-seeding with on-chip pattern generation and response analysis that can be stored on-chip or applied from external sources
- Diagnosis using MISR signature analysis supported for manufacturing test using TestMAX Diagnosis

Traditional and X-tolerant logic BIST

Standard logic BIST requires designs to be free of unknown (i.e., X) simulation values for correct operation. However, with aggressive design practices and new technologies, predicting post-silicon logic values is challenging when considering factors such as sophisticated fault models, design initialization, timing marginalities, and operating parameter variations.

TestMAX XLBIST performs optimally on X-clean designs but provides the ability to handle designs with X values via selective masking of scan chains. This ability ensures that self-test will operate on the manufactured device with little impact to the operational time and fault coverage for most scenarios.

Deterministic ATPG compression supported with XLBIST logic

The TestMAX XLBIST architecture also supports deterministic pattern generation with TestMAX ATPG, eliminating the need for separate codec logic and additional area overhead. TestMAX XLBIST also has the ability to generate hardware to enable power-aware patterns that limits switching activity for both self-test and deterministic pattern generation modes.

X-tolerant logic BIST pattern generation

With the ability to re-seed the pseudo-random pattern generator (PRPG), dynamic x-tolerant logic, and lower power sequencer in an automatic, intelligent manner, TestMAX XLBIST achieves significant increases in fault coverage in less time compared to traditional logic BIST solutions. Figure 2 shows an example comparison of coverage versus pattern count for a given number of pattern seeds.
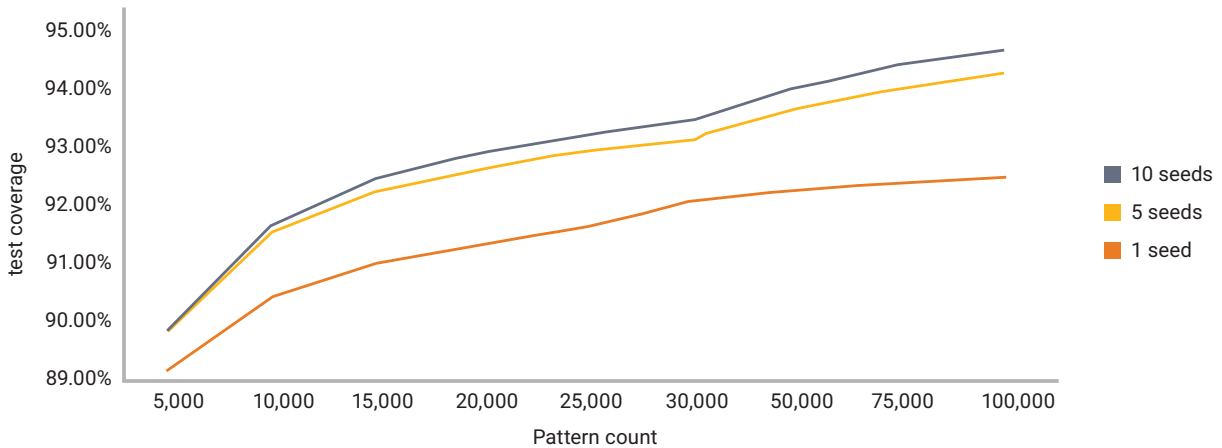

Figure 2: TestMAX XLBIST achieves high coverage with multiple seeds

Since the number of bits required for a seed and associated response is in the order of 100s of bits, TestMAX XLBIST supports multiple seeds stored on-chip for in-system test or supplied externally.

Design Formats

TestMAX XLBIST supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Assertions: OVL, SV
- Verification: SAIF, VCD, FSDB

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