



DDR2[®] nVS

nVS Verification Suite

Verification IP

The **DDR2 nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of DDR2 designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their DDR2 compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI** : PCI Express[®]Gen2, PCI-X[™], PCI, SR-IOV
- ☑ **AMBA[®]** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

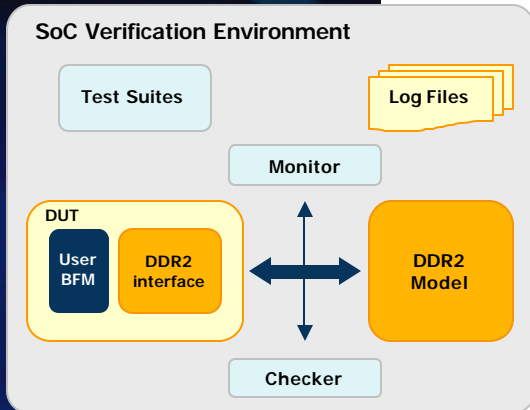
Features

- ◆ Supports DDR2 memory devices from all leading vendors
- ◆ Quickly validates the implementation of the DDR2 standard
- ◆ Constantly monitors DDR2 behavior during simulation
- ◆ Over 110 check-points
- ◆ Check-points include Initialization rules, State based rules, Active Command rules, Read/Write Command rules etc.
- ◆ Support for full-timing as well as behavioral versions in one model
- ◆ Support for all timing delay ranges in one model: min, typical & max

Components

- ◆ DDR2 Memory Models
- ◆ DDR2 Monitor
- ◆ DDR2 Protocol Checker

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster & complete verification of DDR2 designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated DDR2 Verification Suite: Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone DDR2 core or IP verification
- ◆ Verification of SoC with DDR2 interface

Other features

- ◆ Works with industry standard memory models
- ◆ Generates detailed Assertion coverage report
- ◆ On-the-fly protocol & data checking
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Flexible licensing options
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.



nSys Design Systems Pvt. Ltd.
35463 Dumbarton Court Newark CA 94560
Tel: 1-888-nsysinc (1-888-679-7462)
<http://www.nsysinc.com>

**Evaluation
License**

info@nsysinc.com