



DDR3 nVS

nVS Verification Suite

Verification IP

The **DDR3 nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of DDR3 designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their DDR3 compliant designs.

nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

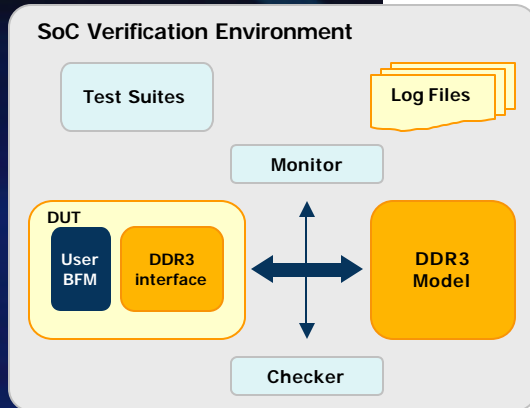
Features

- ◆ Supports DDR3 memory devices from all leading vendors
- ◆ Quickly validates the implementation of the DDR3 standard
- ◆ Supports Double-data-rate architecture; two data transfers per clock cycle
- ◆ Constantly monitors DDR3 behavior during simulation
- ◆ Check-points include Initialization rules, State based rules, Active Command rules, Read/Write Command rules etc.
- ◆ Support for full-timing as well as behavioral versions in one model

Components

- ◆ DDR3 Memory Models
- ◆ DDR3 Monitor
- ◆ DDR3 Protocol Checker

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster & complete verification of DDR3 designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated DDR3 Verification Suite as encrypted/licensed source code
- ◆ User Manual & Application notes
- ◆ Test Suites in source code

Applications

- ◆ Standalone DDR3 core or IP verification
- ◆ Verification of SoC with DDR3 interface

Other features

- ◆ Monitor & Checker are independent modules & can be used with other vendors' memory models
- ◆ Back door access to memory locations
- ◆ Generates detailed Assertion coverage report
- ◆ On-the-fly protocol & data checking
- ◆ Available in Verilog, SystemVerilog
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.