



Ethernet nVS

nSys Verification Suite

Verification IP

The **Ethernet nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of 100/ 40/ 10/ 1G Ethernet interface designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their Ethernet compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI™ Family** : PCI Express®Gen3/Gen2/Gen1, SR-IOV, PCI-X™, PCI™
- ☑ **Communications**: Ethernet (100/40/10/1G), Interlaken, SPI 4.2
- ☑ **Consumer**: USB 3.0, USB 2.0
- ☑ **Storage**: SAS, SATA 3.0, ATAPI
- ☑ **ARM AMBA®** : AXI, AHB, APB
- ☑ **Memory**: DDR3, DDR2
- ☑ **Others**: SDIO, I2C, UART, SMBus, PCMCIA, ASI, IEEE1284 ...

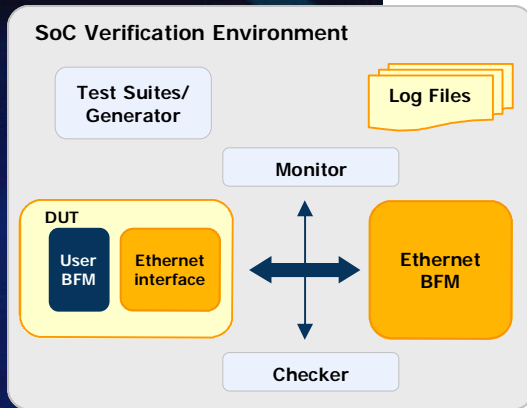
Features

- ◆ Compliant to IEEE 802.3az
- ◆ Support for GMII & XGMII interfaces
- ◆ Support for XSBI/10GBase-R/KR, XAUI/XGXS/10GBase-X/KX4, XFBI, TBI/KX, SGMII interfaces
- ◆ Support for **Auto-Negotiation** (clause 73 & 37)
- ◆ Support for **FEC** (clause 74) and **Rate Adaptation** (clause 72)
- ◆ Full/Half (1G) Duplex Flow Control support
- ◆ Supports frame types: Data, Control Pause & VLAN to frame
- ◆ Automatic re-transmission of Control Pause frame
- ◆ Link State Fault generation mechanism
- ◆ Supports collision scenarios and implements back-off algorithms (1G)

Components

- ◆ Ethernet MAC BFM
- ◆ Ethernet PHY BFM
- ◆ Ethernet Checker
- ◆ Ethernet Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Constrained Random tests
 - Compliance (UNH - IOL) (optional)
 - Functional Coverage tests (optional)

World's largest portfolio of Verification IPs



Key benefits

- ◆ Coverage Driven Verification
- ◆ Faster & complete verification of Ethernet designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated Ethernet Verification Suite: BFMs, Monitor, Checker
- ◆ Compliance Test Suite in source code (optional)
- ◆ User Manual & Application notes

Applications

- ◆ Standalone Ethernet core or IP verification
- ◆ Verification of SoC with Ethernet interface

Other features

- ◆ Generates & drives bus traffic
- ◆ Extensive configurability based on implementation specifics
- ◆ Easy integration & efficient debugging features
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Option for SystemVerilog (OVM/VMM) & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that accelerate designs of customers developing ASIC/SoC, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/SoC developers worldwide are using the nVS family & benefitting from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS family enables users to quickly build environments to verify their designs at system as well as block level.