



I²C[®] nVS

nVS Verification Suite

Verification IP

The **I²C nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of I²C designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their I²C compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI** : PCI Express[®]Gen2, PCI-X[™], PCI, SR-IOV
- ☑ **AMBA[®]** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

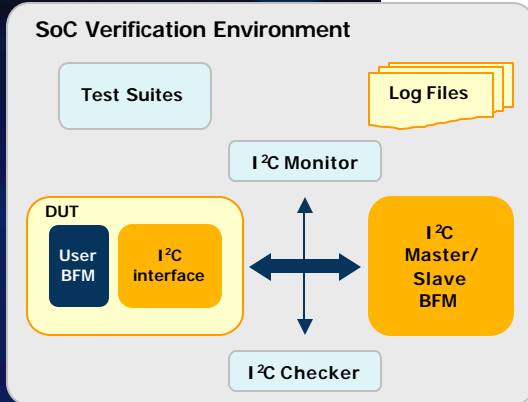
Features

- ◆ Fully compliant with version 2.1 of the Philip's I²C -Bus Specification
- ◆ Support for all types of I²C devices:
 - Master
 - Slave
- ◆ Support for all three I²C bus speeds (High speed Mode, Fast Mode, Standard Mode)
- ◆ Support for 7/10 bit slave addressing
- ◆ Generation of Start, Stop & Repeated Start conditions
- ◆ Slave can be configured as a Generic I²C or I²C EEPROM Slave
- ◆ Data integrity checking in case of I²C EEPROM Slave

Components

- ◆ I²C Master/Slave BFM
- ◆ I²C Checker
- ◆ I²C Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - User Specified tests

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster & complete verification of I²C designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated I²C Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone I²C core or IP verification
- ◆ Verification of SoC with I²C interface

Other features

- ◆ Generates & drives bus traffic as a I²C Master
- ◆ Responds to transactions as a I²C Slave
- ◆ Protocol checks for I²C compliant Master/Slave
- ◆ Support for Multi Master environment to check arbitration logic
- ◆ Simple & flexible BFM tasks
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.