



# IEEE 1284<sup>®</sup> nVS

nVS Verification Suite

Verification IP

The **IEEE 1284 nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of IEEE 1284 designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their IEEE 1284 compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

## Features

- ◆ Fully compatible with IEEE 1284
- ◆ ECP, EPP 1.7, EPP 1.9, SPP, PS2, & Buffered SPP modes supported
- ◆ DMA operations supported
- ◆ Decompression supported
- ◆ Auto-negotiation to ECP, Byte & Nibble
- ◆ On-the-fly protocol & data checking
- ◆ Support for multiple instantiations to create complex verification environment

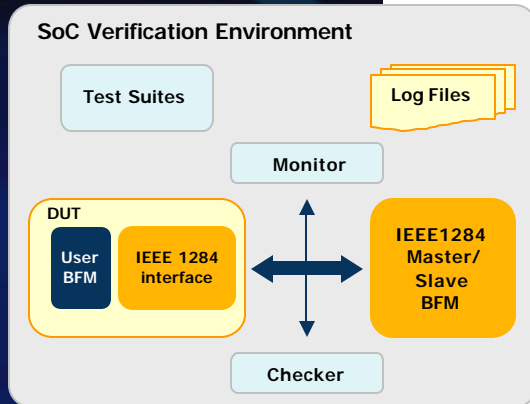
## nVS family

- ☑ **PCI** : PCI Express<sup>®</sup>Gen2, PCI-X<sup>™</sup>, PCI, SR-IOV
- ☑ **AMBA<sup>®</sup>** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I<sup>2</sup>C, SMBus, ASI, PCMCIA, IEEE1284

## Components

- ◆ IEEE 1284 Master BFM
- ◆ IEEE 1284 Slave BFM
- ◆ IEEE 1284 Checker
- ◆ IEEE 1284 Monitor
- ◆ Test Suites
  - Basic tests
  - Error tests
  - Directed tests
  - Constrained Random tests
  - User Specified tests

**World's largest portfolio of Verification IPs**



## Key benefits

- ◆ Faster & complete verification of IEEE 1284 designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

## Deliverables

- ◆ Validated IEEE 1284 Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

## Applications

- ◆ Standalone IEEE 1284 core or IP verification
- ◆ Verification of SoC with IEEE 1284 interface

## Other features

- ◆ Generates & drives bus traffic as a IEEE 1284 Master
- ◆ Responds to transactions as a IEEE 1284 Slave
- ◆ Mailboxes for data checking
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Available in OpenVera
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

## Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

## About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

## About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.