

Independent Verification Services

Increasing complexity of ASICs has offset the advances made in Verification technology. As a result, Verification consumes more than 50% of the development effort, and yet 82% of the designs with re-spins resulting from logic/functional flaws had design errors. This clearly indicates that significant corner cases were ignored in the verification process.

nSys helps Accelerate designs by providing an independent interpretation of the specifications to help reduce the bugs in a design at a faster pace.

Independent Verification while greatly increasing the possibilities of success helps upto 40% faster time-to-market.

Services

- ASIC/ FPGA/ IP Design services**
- Independent Verification services**
- SystemVerilog Migration services**
- Post Silicon Validation services**

Why nSys?

- ◆ Extensive experience in providing product development services in the area of ASIC/ FPGA/IP design & verification
- ◆ Proven expertise and processes for independent verification
- ◆ Leverage nSys Verification Suite (nVS) family, the world's largest portfolio of Verification IPs
- ◆ Extensive know-how of a wide range of high-level verification languages & methodologies: SystemVerilog, SystemC, OpenVera
- ◆ Transparent Project Management
- ◆ User friendly project portal
- ◆ Flexible business models
- ◆ Ability to deploy resources at a very short notice

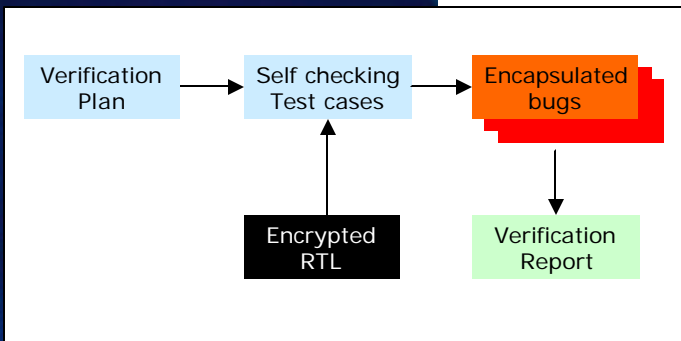
Capabilities

- ◆ Verification Methodology development
- ◆ Verification Plan development
- ◆ Coding Self-checking Test cases
- ◆ End-to-end Checker development
- ◆ Development of Custom VIP/ Assertion Checkers
- ◆ Test case execution and analysis
- ◆ Verification report generation

World's largest portfolio of Verification IPs

Independent Verification Services

Sample Flow:



Sample Projects:

Independent Verification of:

- PCI Express to PCI Bridge
- PHY
- PCI Express IP

Key Benefits

- ◆ Significant improvement in Verification productivity
- ◆ Find more bugs faster
- ◆ Customer focus on design only
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Verification Plan
- ◆ Verification report
- ◆ Source code of Testbenches
- ◆ Test Suites
- ◆ Scripts
- ◆ Verification IPs

Applications

- ◆ Standalone core or IP verification
- ◆ Verification of ASIC/ SoC/ FPGA

Key Milestones

- ◆ Customer Requirement Specifications
- ◆ Project Development Plan
- ◆ Verification Plan
- ◆ Verification Plan joint review
- ◆ Build Test Environment & Test cases
- ◆ Execute Verification Plan
- ◆ Acceptance Plan
- ◆ Acceptance Plan joint review
- ◆ Acceptance

About nSys

nSys is the leading provider of Verilog and VHDL based Verification IPs. nSys provides products & services to Accelerate Designs of its customers, by focusing on the verification phase of ASIC development.

About nVS family

nSys Verification Suite (nVS) family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA/IP developers in over 10 countries are currently using the nVS family and benefit from widely accepted & proven Bus Function Models, Monitors, Assertions-based Checkers and Test Suites for standard interfaces/protocols, that enable users to quickly build environments to verify their designs at system as well as block levels.



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**For
Proposal**

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