

CASE STUDY

INDEPENDENT VERIFICATION SERVICES

THE CUSTOMER

A Silicon Valley-headquartered world leader in developing and delivering semiconductor products for standards-based serial switching.

BUSINESS NEED

In June 2005, while the PCIe chip development stages were being planned by the client, they decided to go in for a third-party Independent Verification service so that internal resources could focus on the design.

The client had already invested in a commercial VIP solution, but due to resource crunch, design complexity and time constraints, it decided to get verification done independently.

THE CHALLENGES

- Make the design bug-free at a fixed cost, rather than on time and material.
- The entire project had to be completed within 6 months.
- The design was undergoing changes all the while.
- The project required strong competence in PCIe, PCI-X, system knowledge & verification methodology.

THE SOLUTION

nSys was chosen as the vendor for Accelerating design. The inputs given to nSys were the detailed specifications & encrypted RTL design.

"I never thought I'd say this, but please stop filing any new bugs until we give you a "green light", which will take at least a week. Filing new bugs at this point will simply overwhelm our team and has already overflowed our disk space. We need some time without new bugs to "dig out from under the rubble"!!.

Verification Manager

nSys adopted the approach of making each bug a deliverable, so that it could be independently re-created by the design team.

Verification Environment

The first step was to set up the environment:

- The Bug Tracking System that would be used by the client's design team and the nSys verification team was identified.
- The process was clearly defined between the two teams regarding directory structure, tagging the database, setting up of secured FTP accounts, and how the data would be transferred to and fro.
- The client had an exact replica of the verification environment at their end.
- The verification environment was completely automated, even the bug database tarball was automatically created and uploaded.

Verification Plan

nSys developed an exhaustive Verification Plan that included Basic, Directed, Random and Compliance Test Suites. It also included short and long regressions. After the team at nSys had internally reviewed the Verification Plan, a joint review of the Verification Plan was done with the client.

Test cases and execution

- The test cases coded to implement the Verification Plan were self-checking.
- Each bug database was sent to the client in a single tarball as an "Encapsulated Bug" consisting of the design, Verification IPs, dump-file, log files and test-bench.
- Client could use the "Encapsulated Bug" to easily replicate the bug at their end, fix it and then use short regressions provided by nSys before checking-in the design.
- The nSys team kept finding bugs in other areas of the design while the client was fixing the bugs already reported.

SUMMARY

The nSys team completed the Independent Verification in a short span of 6 months.

The best comment summing up the entire relationship dynamics, coming from the client was, **"nSys was like an Oasis for us in the entire project"**.

We could hardly ask for more!

KEY BENEFITS

- **Improved cost savings:** As the nSys team was well-versed with most interfaces on the chip being designed, they hit the ground running. The study phase required the reading of the chip specs only, resulting in significant cost savings.
- **Optimized resource utilization:** Client team was able to focus completely on design.
- **Significant improvement in verification productivity:** Since the team at nSys was well-versed in using their own tools, they could leverage them to find bugs much faster than was anticipated by the client.
- **Going beyond the requirements:** nSys verification team was able to uncover bugs that were missed in the verification of the previous generation of the design.

About nSys

nSys leverages the world's largest portfolio of Verification IPs to provide products & services to Accelerate Designs for its customers developing ASIC, FPGA or IP.

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