



# nVS for PCI-X®

nVS Verification Suite

Verification IP

The **nVS for PCI-X** is a comprehensive Verification IP solution for pre-silicon functional verification of PCI-X designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their PCI-X compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

## Features

- ◆ Supports PCI-X Bus Specification Revision 1.0
- ◆ Supports PCI-X mode 1 & mode 2
- ◆ Provides error injection with a wide variety of error types
- ◆ Scalable architecture for use as a standalone test environment or embedding in an SoC environment
- ◆ On-the-fly protocol & data checking
- ◆ Support for multiple instantiations to create complex verification environment

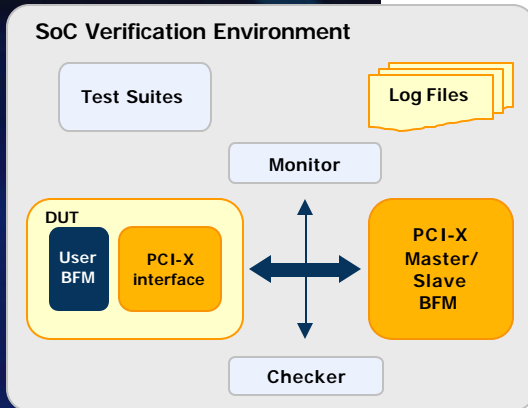
## nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

## Components

- ◆ PCI-X Master/Target BFM
- ◆ PCI-X Checker
- ◆ PCI-X Monitor
- ◆ Test Suites
  - Basic tests
  - Error tests
  - Directed tests
  - Constrained Random tests
  - Compliance tests
  - User Specified tests

**World's largest portfolio of Verification IPs**



## Key benefits

- ◆ Faster & complete verification of PCI-X designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

## Deliverables

- ◆ Validated PCI-X Verification Suite: BFM, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

## Applications

- ◆ Standalone PCI-X core or IP verification
- ◆ Verification of SoC with PCI-X interface

## Other features

- ◆ Generates all types of PCI-X transactions as a PCI-X Master & responds as a PCI-X target
- ◆ Supports memory modeling of all types of memory spaces (configuration/IO/ Memory)
- ◆ Supports 32-bit & 64-bit transactions
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

## Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

## About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

## About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.



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