



nVS for PCI®

nVS Verification Suite

Verification IP

The **nVS for PCI** is a comprehensive Verification IP solution for pre-silicon functional verification of PCI designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their PCI compliant designs.

Availability of Test Suites enables the designers to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

Features

- ◆ Compliant to PCI 2.3 specification
- ◆ Supports 32/64 bit address/data
- ◆ Supports back to back cycles
- ◆ Provides error injection with a wide variety of error types
- ◆ Scalable architecture for use as a standalone test environment or embedding in an SoC environment
- ◆ On-the-fly protocol & data checking
- ◆ Support for multiple instantiations to create complex verification environment

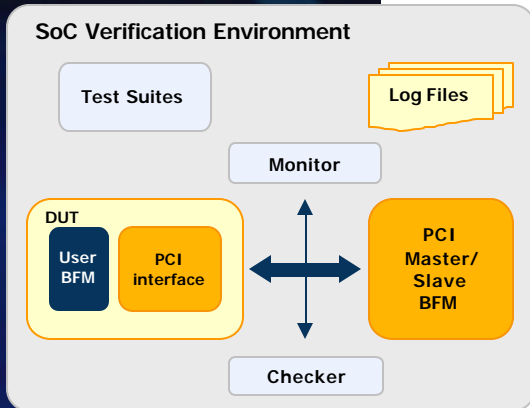
nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

Components

- ◆ PCI Master/Target BFM
- ◆ PCI Checker
- ◆ PCI Monitor
- ◆ PCI Arbiter
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - Compliance tests

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster & complete verification of PCI designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated PCI Verification Suite: BFM, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone PCI core or IP verification
- ◆ Verification of SoC with PCI interface

Other features

- ◆ Generates all types of PCI transactions as a Master
- ◆ Responds to all types of PCI transactions as a Target
- ◆ Supports memory modeling of all memory spaces (configuration/IO/ Memory)
- ◆ Plug-n-Play solution
- ◆ Easy to integrate in any environment
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.



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**Evaluation
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