



nVS for PCIe®

Gen3/ Gen2/ Gen1
nSys Verification Suite

Verification IP

The **nVS for PCI Express®** is one of the most widely accepted & proven solutions for functional verification of PCI Express designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their PCI Express compliant designs.

Availability of Test Suites including, **nSys compliance tests**, enables the designer to focus on features unique to their design, and to verify their differentiators easily. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI™ Family** : PCI Express®Gen3/Gen2/Gen1, SR-IOV, PCI-X™, PCI™
- ☑ **Communications**: Ethernet (100/40/10/1G), Interlaken, SPI 4.1
- ☑ **Consumer**: USB 3.0, USB 2.0
- ☑ **Storage**: SAS, SATA 3.0, ATAPI
- ☑ **ARM AMBA®** : AXI, AHB, APB
- ☑ **Memory**: DDR3, DDR2
- ☑ **Others**: SDIO, I2C, UART, SMBus...

Features

- ◆ Proven support for all types of PCI Express devices: Endpoints , Root Complex, Switch
- ◆ Backward compatibility with Gen2/Gen1
- ◆ Flexibility to send completely automated packets or completely user configured packets in all the three layers
- ◆ Ability to inject errors for packets being generated in all the three layers
- ◆ Supports Speed Negotiation and Link width Up-Configuration
- ◆ On-the-fly protocol & data checking/ score board
- ◆ **Available in native SystemVerilog (OVM/VMM) & Verilog**
- ◆ **Option of Source Code**

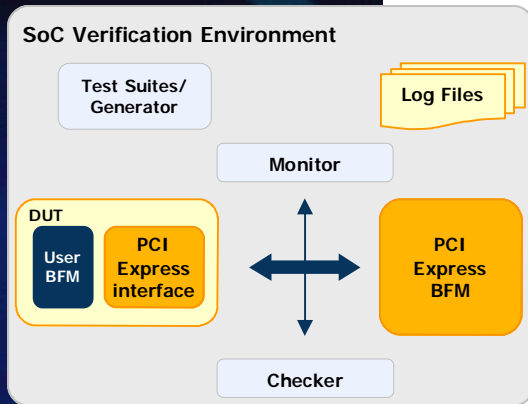
Components

- ◆ PCI Express Requester/Completer BFM
- ◆ PCI Express Checker
- ◆ PCI Express Monitor
- ◆ Test Suites
 - Basic tests
 - Error & Directed tests
 - Constrained Random tests
 - Compliance tests Gen1 (optional)
 - Compliance tests Gen2 (optional)
 - **nSys Compliance tests Gen3 (optional)**
 - **Functional Coverage tests (optional)**

World's largest portfolio of Verification IPs

nVS for PCIe Gen3/ Gen2/ Gen1

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Key benefits

- ◆ Coverage Driven Verification
- ◆ Faster & complete verification of PCI Express designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated PCI Express Verification Suite: BFM, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone PCI Express core or IP verification
- ◆ Verification of SoC with PCI Express interface

Other features

- ◆ Supports PCI Express Specification Revision 3.0, 2.0, 1.1 & 1.0a
- ◆ Responds to transactions as a PCI Express Completer
- ◆ Implements PCI Express configuration space as well as PCI Express Advanced Error Reporting Capabilities register
- ◆ LTSSM Coverage report generation
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Support for Auto Enumeration
- ◆ Consistency of interface, installation, operation & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the World's Largest Portfolio of Verification IPs to provide products and services that Accelerate designs of customers developing ASIC/ SoC, while lowering their costs & risks.

About nVS

nVS (nSys Verification Suite) family of VIPs is integrated to work with popular languages, like, 'e', SystemC, OpenVera, VHDL, on all commonly used simulators/platforms. nVS is a complete Verification IP solution for pre-silicon Functional Verification of ASIC/SoC designs.



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**Product
Evaluation**

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