



SAS® nVS

nSys Verification Suite

Verification IP

The **SAS nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of SAS designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their SAS compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI™ Family** : PCI Express®Gen3/Gen2/Gen1, SR-IOV, PCI-X™, PCI™
- ☑ **Communications**: Ethernet (100/40/10/1G), Interlaken, SPI 4.1
- ☑ **Consumer**: USB 3.0, USB 2.0
- ☑ **Storage**: SAS, SATA 3.0, ATAPI
- ☑ **ARM AMBA®** : AXI, AHB, APB
- ☑ **Memory**: DDR3, DDR2
- ☑ **Others**: SDIO, I2C, UART, SMBus...

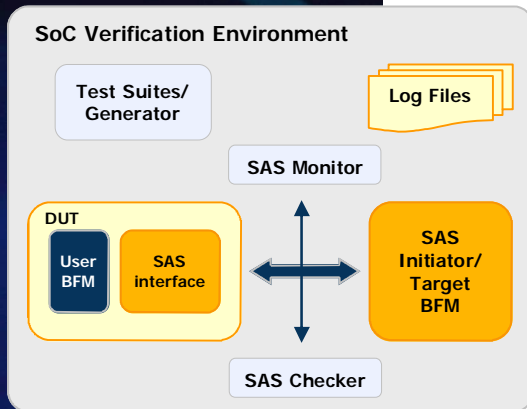
Features

- ◆ Supports SAS-2 Specification Revision 16
- ◆ Support for all types of SAS devices:
 - Initiator
 - Target
 - Expander
- ◆ Full support of SSP, SMP & STP protocols
- ◆ Support for Wide ports
- ◆ Support for Multiplexing
- ◆ Provides error injection with a wide variety of error types
- ◆ **Available in native SystemVerilog (OVM/VMM) & Verilog**
- ◆ **Option of Source Code**

Components

- ◆ SAS Initiator BFM
- ◆ SAS Target BFM
- ◆ SAS Checker
- ◆ SAS Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - **Functional Coverage tests**

World's largest portfolio of Verification IPs



Key benefits

- ◆ Coverage Driven Verification
- ◆ Faster & complete verification of SAS designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated SAS Verification Suite: BFM, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone SAS core or IP verification
- ◆ Verification of SoC with SAS interface

Other features

- ◆ Generates & drives bus traffic as a SAS Initiator
- ◆ Responds to transactions as a SAS Target
- ◆ Flexibility to send completely automated packets or completely user configured packets in all the layers
- ◆ Mailboxes for data checking
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ On-the-fly protocol & data checking/ score board
- ◆ Support for multiple instantiations to create complex verification environment
- ◆ Consistency of interface, installation, operation & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the World's Largest Portfolio of Verification IPs to provide products and services that Accelerate designs of customers developing ASIC/ SoC, while lowering their costs & risks.

About nVS

nVS (nSys Verification Suite) family of VIPs is integrated to work with popular languages, like, 'e', SystemC, OpenVera, VHDL, on all commonly used simulators/platforms. nVS is a complete Verification IP solution for pre-silicon Functional Verification of ASIC/SoC designs.