

# Serial ATA® nVS

nSys Verification Suite

Verification IP

The **SATA nVS** is a comprehensive Verification IP solution for functional verification of Serial ATA designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their Serial ATA compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design, and to verify their differentiators easily. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

## nVS family

- ☑ **PCI™ Family** : PCI Express®Gen3/Gen2/Gen1, SR-IOV, PCI-X™, PCI™
- ☑ **Communications**: Ethernet (100/40/10/1G), Interlaken, SPI 4.1
- ☑ **Consumer**: USB 3.0, USB 2.0
- ☑ **Storage**: SAS, SATA 3.0, ATAPI
- ☑ **ARM AMBA®** : AXI, AHB, APB
- ☑ **Memory**: DDR3, DDR2
- ☑ **Others**: SDIO, I2C, UART, SMBus...

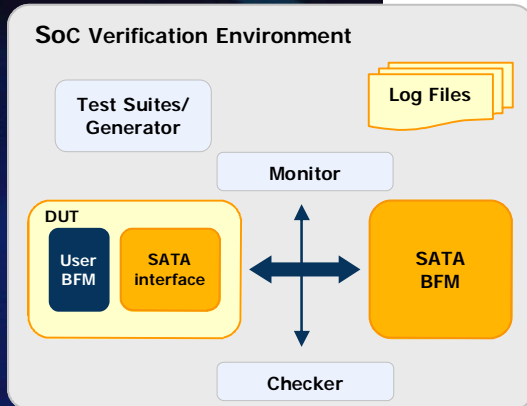
## Features

- ◆ Supports Serial ATA Gen 3.0 specifications
- ◆ Support for all types of Serial ATA devices
  - Host
  - Device
  - Port Multiplier/Port Selector
- ◆ Supports 1-bit, 8-bit, 10-bit, 20-bit, 40-bit or frame level interfaces & all link speeds
- ◆ Supports SAPIs interface
- ◆ Flexibility to send completely automated/user configured packets in all layers
- ◆ **Availability of native SystemVerilog (OVM/VMM) & Verilog**
- ◆ **Option of Source Code**

## Components

- ◆ Serial ATA Host BFM
- ◆ Serial ATA Device BFM
- ◆ Serial ATA Checker
- ◆ Serial ATA Monitor
- ◆ Test Suites
  - Basic tests
  - Error tests
  - Directed tests
  - Constrained Random tests
  - **Compliance Tests (optional)**
  - **Functional Coverage Tests (optional)**

**World's largest portfolio of Verification IPs**



## Key benefits

- ◆ Coverage Driven Verification
- ◆ Faster & complete verification of Serial ATA designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

## Deliverables

- ◆ Validated Serial ATA Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

## Applications

- ◆ Standalone Serial ATA core or IP verification
- ◆ Verification of SoC with SATA interface (Host/Device/Port Multiplier)

## Other features

- ◆ Generating & driving bus traffic as a Serial ATA Host
- ◆ Responding to transactions as a Serial ATA Device
- ◆ Mailboxes for data checking
- ◆ Full support for automatic random, directed & error testing
- ◆ On-the-fly protocol & data checking
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Flexibility to send fully automated configurable response
- ◆ Ability to inject errors in packets being generated in all the three layers
- ◆ Consistency of interface, installation, operation & documentation across nVS family

## Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

## About nSys

nSys offers the World's Largest Portfolio of Verification IPs to provide products and services that Accelerate designs of customers developing ASIC/ SoC, while lowering their costs & risks.

## About nVS

nVS (nSys Verification Suite) family of VIPs is integrated to work with popular languages, like, 'e', SystemC, OpenVera, VHDL, on all commonly used simulators/platforms. nVS is a complete Verification IP solution for pre-silicon Functional Verification of ASIC/SoC designs.