



# SDIO® nVS

nSys Verification Suite

Verification IP

The **SDIO nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of SDIO (Secure Digital I/O) designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their SDIO compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

## nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

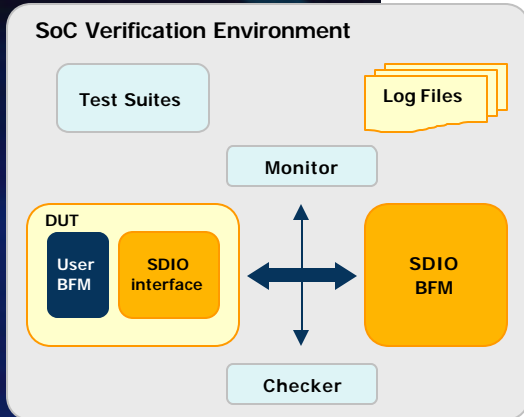
## Features

- ◆ Supports SDIO Bus Specification Version 2.0
- ◆ Supports SPI, 1-bit SD & the 4-bit SD transfer modes at the full clock range of 0-50 MHz
- ◆ Support for all types of SDIO devices:
  - Host
  - Card
- ◆ Provides error injection with a wide variety of error types
- ◆ Scalable architecture for use as a standalone test environment or embedding in an SoC environment
- ◆ On-the-fly protocol & data checking
- ◆ Support for multiple instantiations to create complex verification environment

## Components

- ◆ SDIO Host/Card BFM
- ◆ SDIO Checker
- ◆ SDIO Monitor
- ◆ Test Suites
  - Basic tests
  - Error tests
  - Constrained Random tests
  - User Specified tests

**World's largest portfolio of Verification IPs**



## Key benefits

- ◆ Faster & complete verification of SDIO designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

## Deliverables

- ◆ Validated SDIO Verification Suite: BFMs, Monitor, Checker
- ◆ User Manual & Application notes
- ◆ Test Suites in source code

## Applications

- ◆ Standalone SDIO core or IP verification
- ◆ Verification of SoC with SDIO interface

## Other features

- ◆ Generates & drives bus traffic as an SDIO Host
- ◆ Responds to transactions as an SDIO Card
- ◆ Up to 7 functions in SD1, or SD4 mode
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Flexible licensing options
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

## Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

## About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

## About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.