



SMBus® nVS

nVS Verification Suite

Verification IP

The **SMBus nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of SMBus designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their SMBus compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

Features

- ◆ Compliant to SMBus 2.0 specification
- ◆ Generates & drives bus traffic as a SMBus 2.0 Requester
- ◆ Responds to transactions as a SMBus 2.0 Slave
- ◆ Slave is generic & compatible with two wire serial EEPROM
- ◆ Extensive event generation
- ◆ On-the-fly protocol & data checking
- ◆ Support for multiple instantiations to create complex verification environment

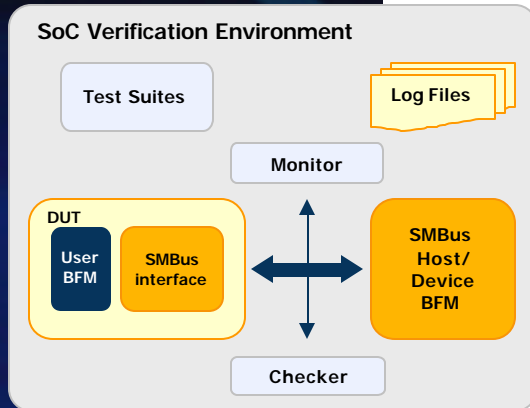
nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

Components

- ◆ SMBus Master/Slave BFM
- ◆ SMBus Checker
- ◆ SMBus Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - User Specified tests

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster & complete verification of SMBus designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated SMBus Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone SMBus core or IP verification
- ◆ Verification of SoC with SMBus interface

Other features

- ◆ Support Write & Read data interleaving
- ◆ Responds to transactions as a SMBus
- ◆ Mailboxes for data checking
- ◆ Checker generates detailed Assertion coverage report
- ◆ Highly parameterized: Verification environment & logical parameters
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.