



nVS for SR-IOV®

nSys Verification Suite

Verification IP

The **nVS for SR-IOV®** is built upon nVS for PCI Express®, one of the most widely accepted & proven solutions for functional verification of PCI Express designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their SR-IOV enabled designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI** : PCI Express®Gen2, PCI-X™, PCI, SR-IOV
- ☑ **AMBA®** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

Features

- ◆ Built upon nVS for PCIe Gen2
- ◆ Support for Physical Function (PF) and Virtual Function (VF) Configuration Spaces
- ◆ IOV resource discovery & configuration
- ◆ Supports Function Level Reset (FLR)
- ◆ Supports Address Translation Services
- ◆ Flexibility to send completely automated packets or completely user configured packets in all the three layers
- ◆ Ability to inject errors for packets being generated in all the three layers
- ◆ Support for all Link widths & PHY interfaces
- ◆ Support for multiple instantiations to create complex verification environment

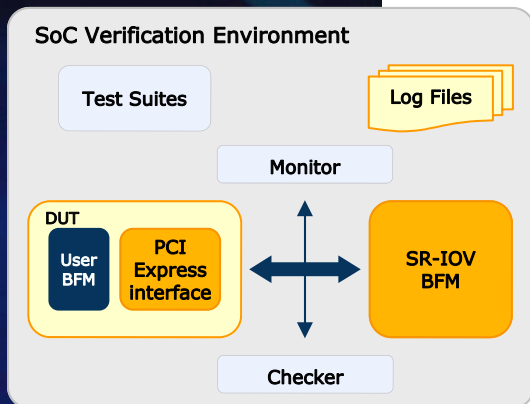
Components

- ◆ SR-IOV Requester/Completer BFM
- ◆ Checker
- ◆ Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - Compliance tests (optional)

World's largest portfolio of Verification IPs

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Key benefits

- ◆ Faster & complete verification of SR-IOV enabled PCI Express designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated SR-IOV Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone SR-IOV core or IP verification
- ◆ Verification of SR-IOV SoC with PCI Express interface

Other features

- ◆ Supports PCI Express Base Specification Revision 2.0, 1.1 & SR-IOV
- ◆ Responds to transactions as a PCI Express Completer
- ◆ Implements PCI Express configuration space as defined for End Points, PCI Express Extended Capabilities, PCI Express Advanced Error Reporting Capabilities as well as SR-IOV Extended Capabilities
- ◆ Fully Automated Flow Control
- ◆ Option for SystemVerilog (OVM/VMM) & Verilog
- ◆ **Option for Source code licenses**
- ◆ Consistency of interface, installation, operation & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.



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**Product
Demo**

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