



USB 3.0 nVS

nSys Verification Suite

Verification IP

The **USB 3.0 nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of USB designs. The USB 3.0 nVS builds upon the widely used nVS for PCIe® and the USB 2.0 nVS.

The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their USB 3.0 compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design, and to verify their differentiators easily. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI™ Family** : PCI Express®Gen3/Gen2/Gen1, SR-IOV, PCI-X™, PCI™
- ☑ **Communications**: Ethernet (100/40/10/1G), Interlaken, SPI 4.1
- ☑ **Consumer**: USB 3.0, USB 2.0
- ☑ **Storage**: SAS, SATA 3.0, ATAPI
- ☑ **ARM AMBA®** : AXI, AHB, APB
- ☑ **Memory**: DDR3, DDR2
- ☑ **Others**: SDIO, I2C, UART, SMBus...

Features

- ◆ Compliant to USB 3.0 Specifications
- ◆ Support for all types of USB models:
 - Host
 - Device
 - Hub
- ◆ Supports serial, serial differential, 10-bit and PIPE interface
- ◆ Provides error injection with a wide variety of error types
- ◆ On-the-fly protocol & data checking/ score board
- ◆ Available in native SystemVerilog (OVM/VMM) & Verilog
- ◆ Option of Source Code

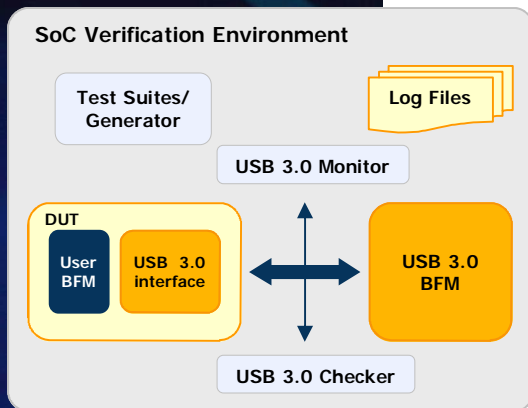
Components

- ◆ USB 3.0 Host/Device BFM
- ◆ USB 3.0 Checker
- ◆ USB 3.0 Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - Functional Coverage tests (optional)
 - USB 3.0 Compliance tests (optional)

World's largest portfolio of Verification IPs

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Key benefits

- ◆ Coverage Driven Verification
- ◆ Faster & complete verification of USB 3.0 designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated USB 3.0 Verification Suite: BFMs, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone USB 3.0 core or IP verification
- ◆ Verification of SoC with USB interface

Other features

- ◆ Fully Automated Flow Control
- ◆ Supports Power management
- ◆ Separate transmit & receive clocks for checking DUT's elastic buffer
- ◆ Supports Lane Polarity Inversion
- ◆ Supports Bypassing of Training Sequence, Scrambling
- ◆ Supports Bypassing LFPS during Link Training
- ◆ Generates LTSSM state transition Coverage report
- ◆ Support for Auto Enumeration
- ◆ Consistency of interface, installation, operation & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the World's Largest Portfolio of Verification IPs to provide products and services that Accelerate designs of customers developing ASIC/ SoC, while lowering their costs & risks.

About nVS

nVS (nSys Verification Suite) family of VIPs is integrated to work with popular languages, like, 'e', SystemC, OpenVera, VHDL, on all commonly used simulators/platforms. nVS is a complete Verification IP solution for pre-silicon Functional Verification of ASIC/SoC designs.



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Product
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