



USB[®] nVS

nVS Verification Suite

Verification IP

The **USB nVS** is a comprehensive Verification IP solution for pre-silicon functional verification of USB designs. The nVS allows design & verification engineers to quickly & extensively test the entire functionality of their USB compliant designs.

Availability of Test Suites enables the designer to focus on features unique to their design. The nVS leverages advanced verification techniques in creating a versatile testbench environment.

nVS family

- ☑ **PCI** : PCI Express[®]Gen2, PCI-X[™], PCI, SR-IOV
- ☑ **AMBA[®]** : AXI, AHB, APB
- ☑ **Storage**: SAS, SATA, ATAPI
- ☑ **Communication**: Ethernet, USB 2.0 OTG, SPI 4.2
- ☑ **Memory**: DDR2, DDR3
- ☑ **Display**: MIPI
- ☑ **Others**: SDIO, UART, I²C, SMBus, ASI, PCMCIA, IEEE1284

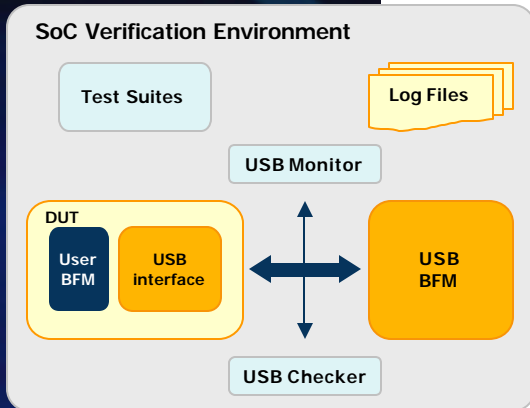
Features

- ◆ Compliant to USB Specification Revision 2.0 (1.1 compatible) & supports OTG supplement to USB 2.0 Revision 1.0a
- ◆ Support for all types of USB models :
 - Host
 - Device
 - Dual-role device
- ◆ Supports D+/D-, UTMI & ULPI interfaces
- ◆ Provides error injection with a wide variety of error types
- ◆ Scalable architecture for use as a standalone test environment or embedding in an SoC environment
- ◆ On-the-fly protocol & data checking

Components

- ◆ USB Host/Device BFM
- ◆ USB Checker
- ◆ USB Monitor
- ◆ Test Suites
 - Basic tests
 - Error tests
 - Directed tests
 - Constrained Random tests
 - User Specified tests
 - Compliance tests

World's largest portfolio of Verification IPs



Key benefits

- ◆ Faster & complete verification of USB designs
- ◆ Significant improvement in Verification productivity
- ◆ Lower rate of failure/ re-spin

Deliverables

- ◆ Validated USB Verification Suite: BFM, Monitor, Checker
- ◆ Test Suites in source code
- ◆ User Manual & Application notes

Applications

- ◆ Standalone USB core or IP verification
- ◆ Verification of SoC with USB interface

Other features

- ◆ Generating & driving bus traffic as a USB Host/Hub
- ◆ Responding to transactions as a USB device
- ◆ Supports SRP & HNP Protocols
- ◆ Supports Bulk, Control, Isochronous & Interrupt Transfer
- ◆ Fully Automated Flow Control
- ◆ Runs at high, full & low speed
- ◆ Highly parameterized Verification environment & logical parameters
- ◆ Available in SystemVerilog & Verilog
- ◆ **Option for Unlimited/Source code licenses**
- ◆ Consistency of interface, installation, operation, & documentation across nVS family

Support

nVS family of Verification IPs is backed by a dedicated team of engineers, trained in advanced verification methodologies, proactively supporting you online through a user friendly portal, on phone & onsite.

About nSys

nSys offers the world's largest portfolio of Verification IPs and leverages services that Accelerate designs of customers developing ASIC/FPGA, while lowering their costs and risks.

About nVS

nVS family is the world's largest portfolio of Verification IPs. Hundreds of ASIC/FPGA developers worldwide are using the nVS family & benefit from the widely accepted & proven Verification IPs for standard interfaces/ protocols. Every nVS consists of BFMs, Monitors, Assertions-based Checkers and Test Suites. nVS' enable users to quickly build environments to verify their designs at system as well as block level.



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**Evaluation
License**

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